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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,609	01/16/2004	Tetsumasa Sato	60675 (48229)	8169

7590 05/27/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,609	SATO, TETSUMASA	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to amended claims 1-4, filed 05/09/2005, have been considered but they are moot in view of new ground(s) of rejection.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming at least one contact layer connected to the resistor layer, a source and a drain in the semiconductor layer simultaneously" of **claim 1** and the "forming a first contact layer connected to the first resistor layer, a second contact layer connected to the second resistor layer, a source and a drain in the semiconductor layer simultaneously" of **claim 2** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Takemoto et al. U.S. Patent 4,233,615 (the '615 reference).

The '615 reference discloses in Figure 3 and respective portions of the specification a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region (29, paragraph 25 of the BACKGROUND OF THE INVENTION Section) and an active region (no number, defined and electrically isolated by the element isolation region), electrically isolated by the element isolation region, on a semiconductor layer (1);

(b) forming a resistor layer (20) in the active region;

(c) forming a gate insulation layer (28') on the semiconductor layer;

(d) forming a gate electrode (30) on the gate insulation layer; and

(e) forming at least one contact layer (16, 17) connected to the resistor layer, a source (14) and a drain (15) in the semiconductor layer simultaneously (paragraph 25 of the BACKGROUND OF THE INVENTION Section).

5. **Claims 1 and 4** are rejected under 35 U.S.C. 102(b) as being anticipated by Robinson et al. European Patent Application Publication 0 545 363 A1 (the '363 reference).

The '363 reference discloses in the figures, particularly Figure 9A, and respective portions of the specification a manufacturing method of a semiconductor device, comprising:

(a) forming an element isolation region (42/17, page 6, lines 32-45) and an active region (7), electrically isolated by the element isolation region, on a semiconductor layer (10);

(b) forming a resistor layer (6, page 7, line 30) in the active region;

(c) forming a gate insulation layer (22) on the semiconductor layer;

(d) forming a gate electrode (25) on the gate insulation layer; and

(e) forming at least one contact layer (8, 8) connected to the resistor layer, a source (33 or 35) and a drain (34 or 36) in the semiconductor layer simultaneously (Figs. 7A and 9A or 8).

Referring to **claim 4**, the figures of the reference clearly depict that the element isolation region (42/17) is semi-recessed LOCOS.

Claim Rejections - 35 USC § 103

6. **Claims 2 and 3** are rejected under 35 U.S.C. §103(a) as being unpatentable over a prior art general semiconductor device or over Thompson U.S. Patent 4,698,530 in view of Robinson et al. European Patent Application Publication 0 545 363 A1 (the '363 reference).

Referring to **claim 2**, a prior art general semiconductor device depicted in Figs. 28-34 of the present application would necessarily include all limitations as recited in steps (a) through (d) of the claim. The prior art general semiconductor device further includes the step of forming a first contact layer (26) connected to the first resistor layer and a second contact layer (26) connected to the second resistor layer. However, the prior art general semiconductor device does not necessarily entail the step of forming these contact layers at the same step for forming a source region and a drain region. In other words, the prior art general semiconductor device fails to explicitly depict the claimed step of forming a first contact layer connected to the first resistor layer, a second contact layer connected to the second resistor layer, a source and a drain in the semiconductor layer simultaneously as required by the claim. The '363 reference, partly detailed above, teaches forming at least one contact layer connected to the resistor layer, a source and a drain in the semiconductor layer simultaneously to obtain a high definition structure (page 4, lines 40-45). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the prior art general semiconductor device by forming the first contact layer connected to the first resistor layer, the second contact layer connected to the second resistor layer, the source and the drain in the semiconductor layer simultaneously. One would have been motivated to make such a change so as to obtain a high definition structure as taught by the '363 reference.

Referring to **claim 3**, the manufacturing method thus modified would necessarily entail, before the step (e) of forming the contact layers, forming a resist layer - such as resist layer 13.0 MASK of Fig. 9A8 and/or mask 23 in Fig. 8 of the '363 reference for a single resistor, modified to accommodate the two resistors of the prior art general semiconductor device - which has a

first opening at least above a termination of the first resistor layer and a second opening at least above a termination of the second resistor layer, the first opening and the second opening being continuous.

In a similar situation, the Thompson's device of a transistor, a first resistor (R31, Fig. 5) and a second resistor (R32) would benefit from the teachings of the '363 reference for obtaining a high definition structure. The Thompson's device thus modified would necessarily entail all the claimed limitations.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
May 20, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800